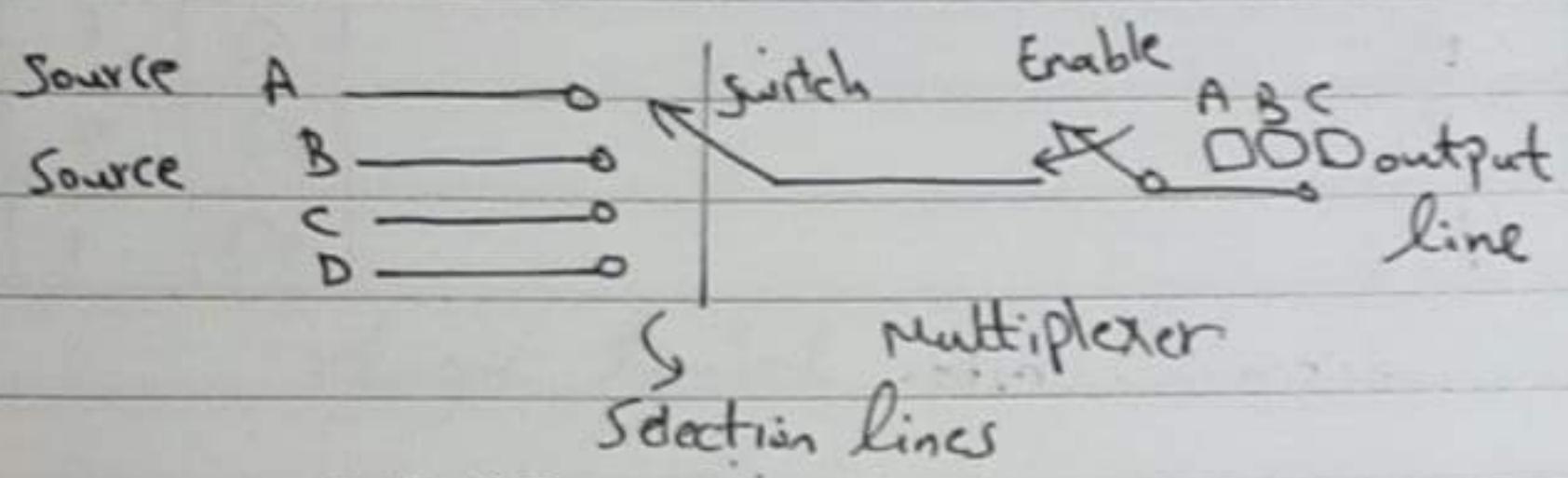


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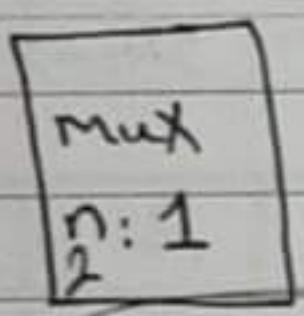
combinational logic Circuit "Data processing Circuits"

*Multiplexer



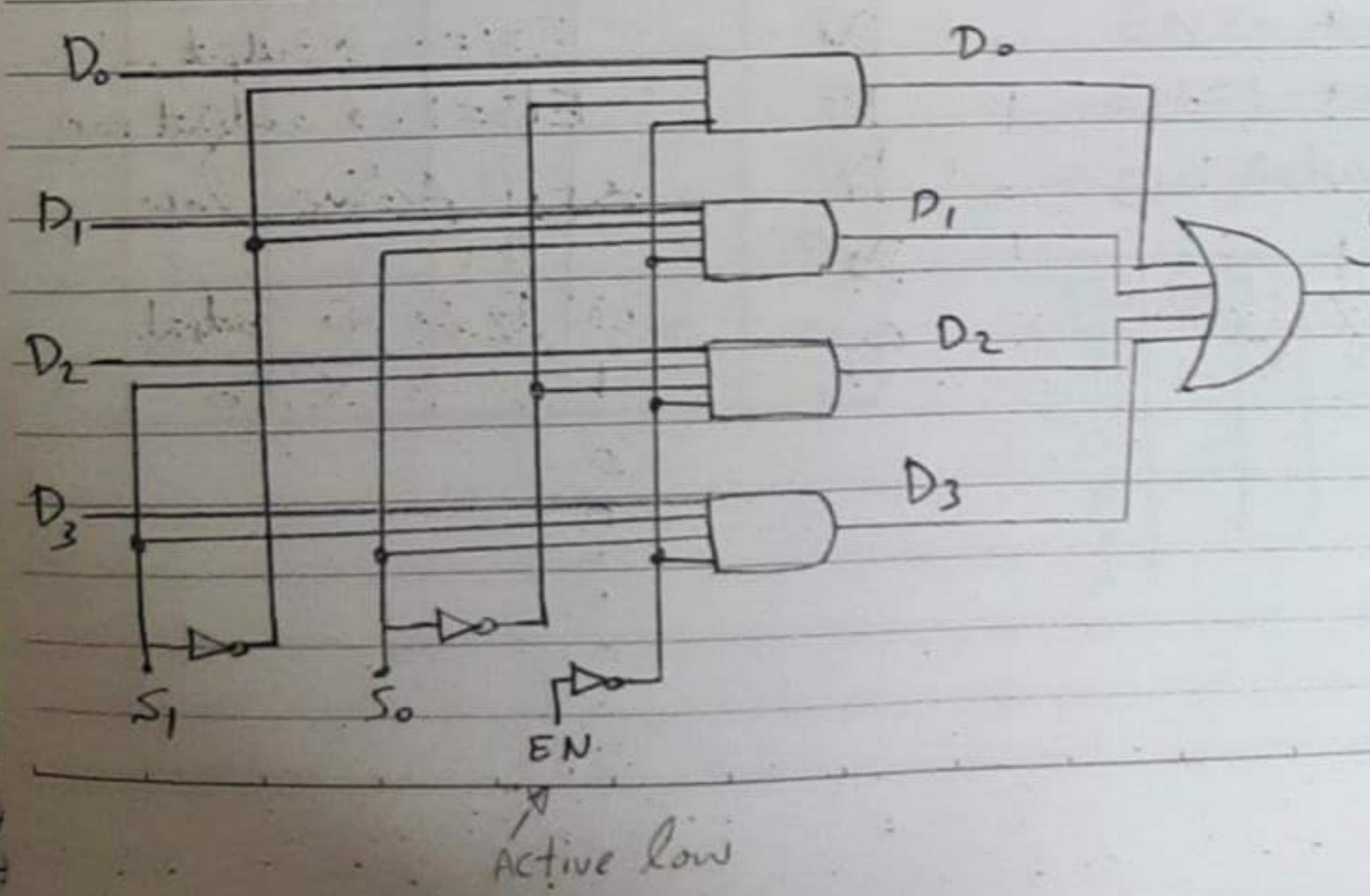
Time Division Multiplexing (TDM) يسمى (TDM) مultiplexer
AND gates are used in multiplexer

number of sources \rightarrow n output $\rightarrow 1$



(input) Sources
4x1 multiplexer → AND gate
(2 selection lines)

Logic Circuit of Mux



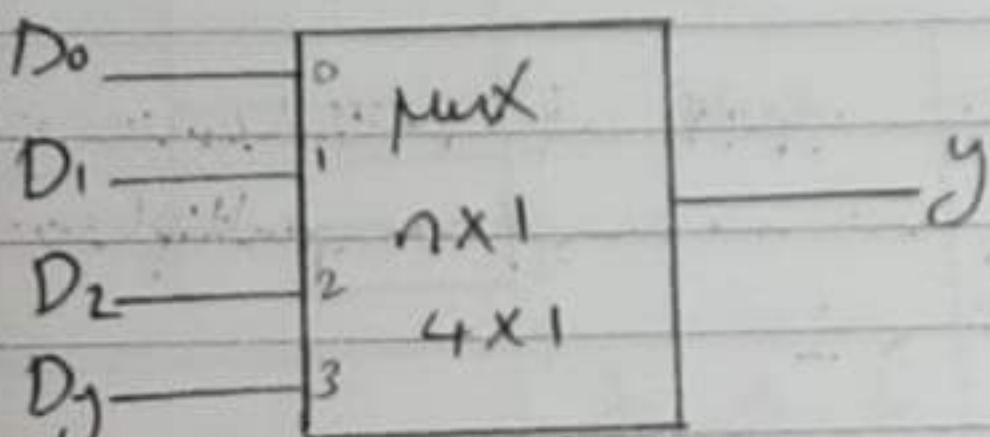
→ 8x1 multiplexer, 3 selector lines

8 → AND gates

* Function table of 4x1 Mux

S_1	S_0	y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

* logic symbol



→ Function table of 8x1 Mux

EN	S_2	S_1	S_0	y
0	0	0	0	D_0
1	0	0	1	D_1
1	0	1	0	D_2
1	0	1	1	D_3
1	1	0	0	D_4
1	1	0	1	D_5
1	1	1	0	D_6
1	1	1	1	D_7
0	X	X	X	0

$EN = 0 \rightarrow \text{output} = 0$

$EN = 1 \rightarrow \text{output} = 1$

* EN Active high

$EN = 0 \rightarrow \text{output} = 1$

$EN = 1 \rightarrow \text{output} = 0$

* EN Active low

EN	S_2	S_1	S_0	add'l
1	X	X	X	0
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0

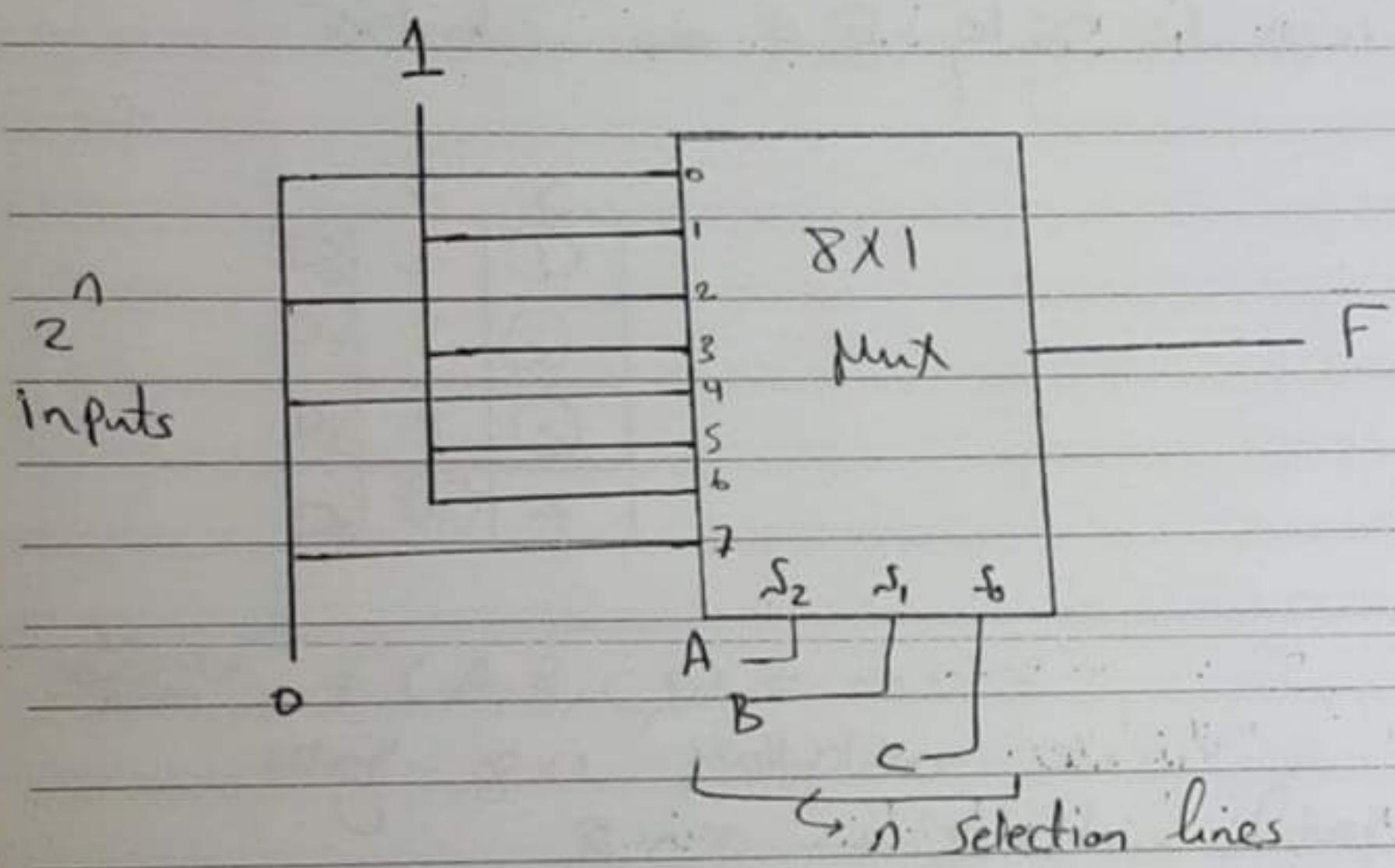
DATE _____
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* $F(A, B, C) = \sum m(1, 3, 5, 6)$ القيمة المطلوبة
مinterm F

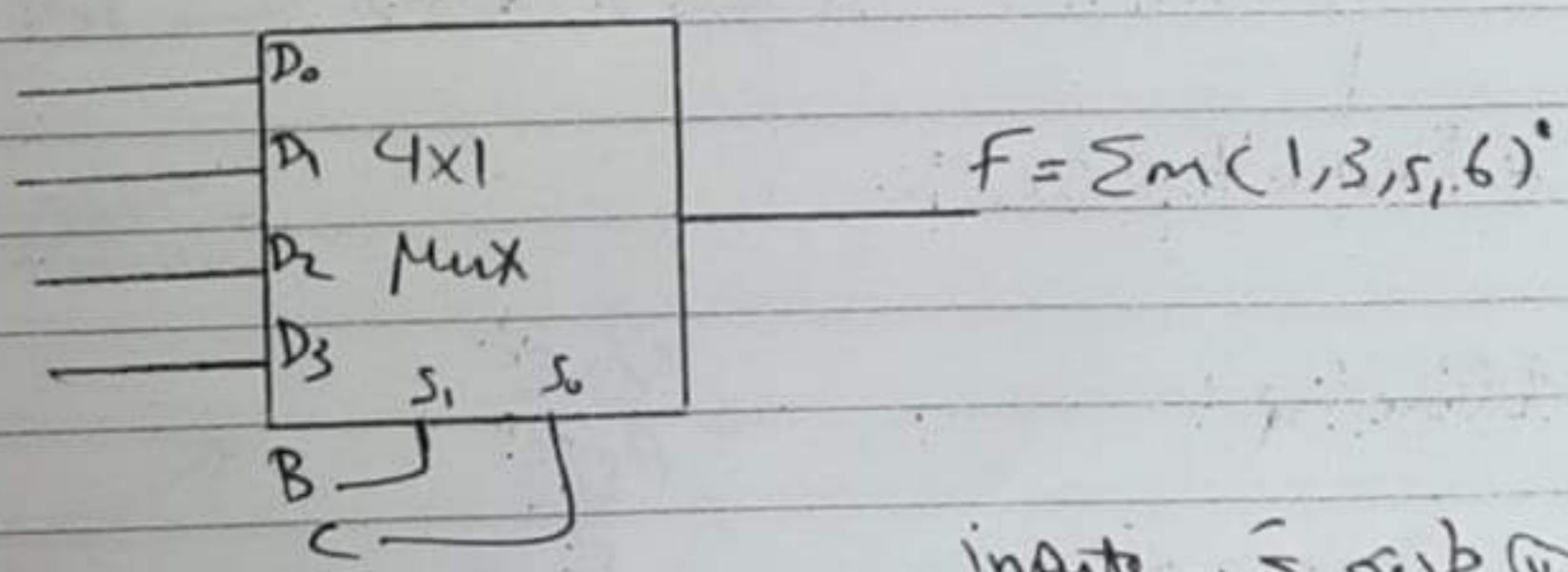
Implement F using 8:1 multiplexer.

$$F(A, B, C) = \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}C + ABC \rightarrow$$

truth table



* Implement the previous function using 4x1 mux.
 اى المطلوب \rightarrow 4x1 mux \rightarrow input \rightarrow selection lines \leftarrow هناك ≥ 2 فقط.



inputs \rightarrow طريقة ④
 minterns ① فتح دائرة لـ \bar{A} \bar{B} \bar{C} المقابل
 ② \bar{A} \bar{B} \bar{C} \rightarrow صنعوا الى عيني \rightarrow وادر.

	D_0	D_1	D_2	D_3
\bar{A}	0	1	2	3
A	4	5	6	7

$$A \leftarrow A \text{ مفهوم المداردة}$$

$$\bar{A} \leftarrow \bar{A} \text{ مفهوم المداردة}$$

Selection $\Leftarrow A, B$ مفهوم المداردة *

	\bar{C}	C
D_0	0	1
D_1	2	3
D_2	4	5
D_3	6	7

مخرج $F(A, B, C, D) = \dots$

using 8x1 Multiplexer

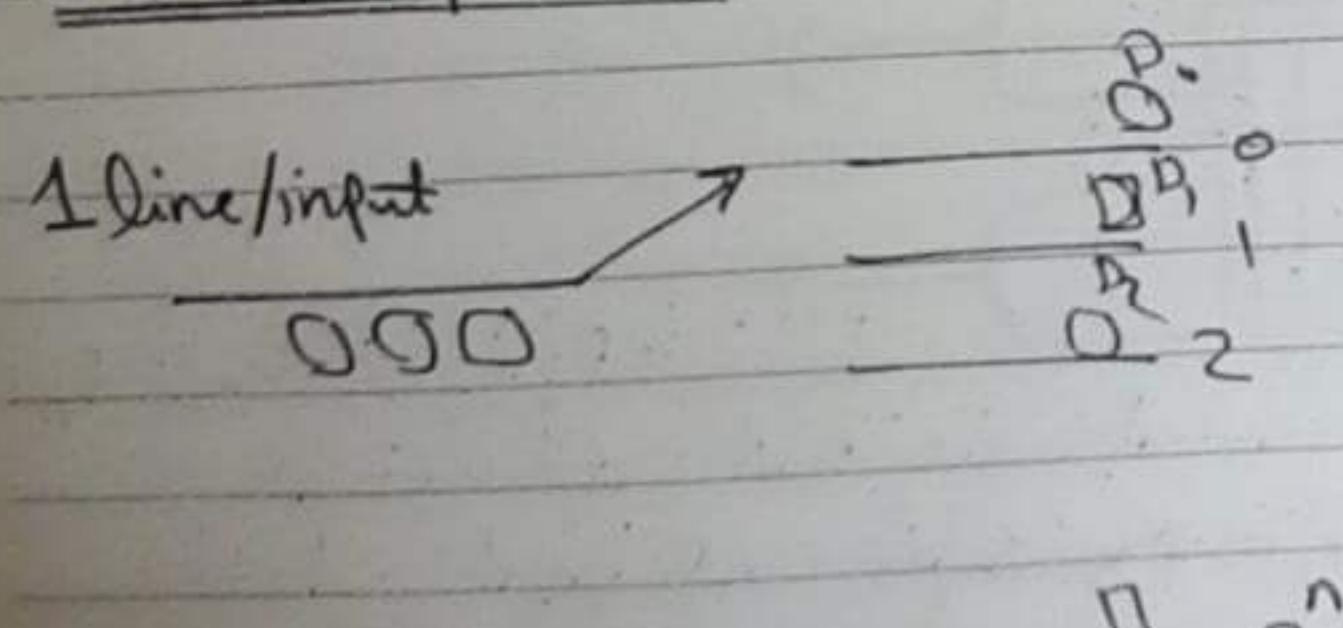
$B, C, D \rightarrow$ selection lines

$A \Rightarrow$ المدخل المختار

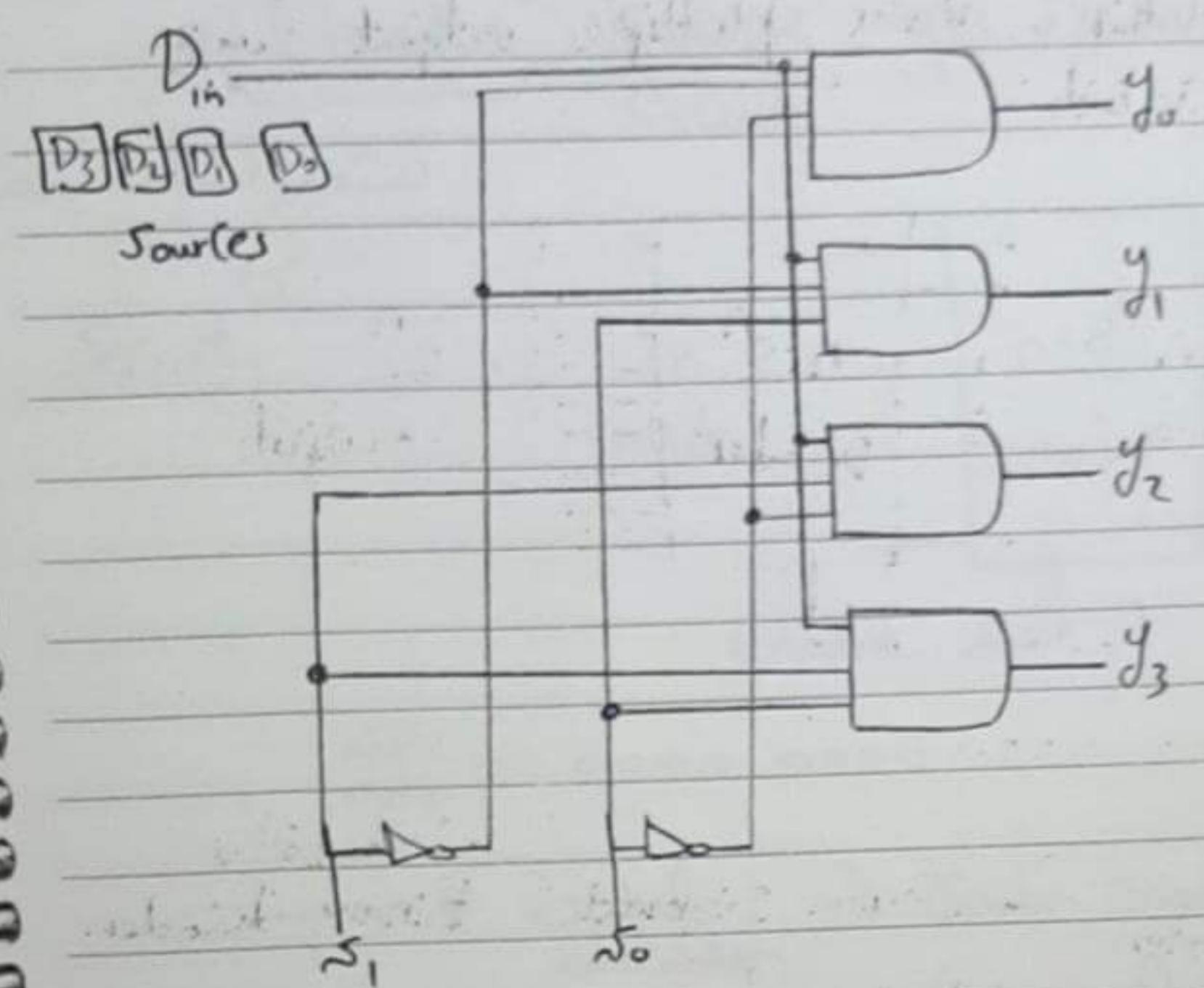
function table multiplexer :- طريقة المداردة

$$74 \times 151 \rightarrow (8 \times 1 \text{ mux})$$

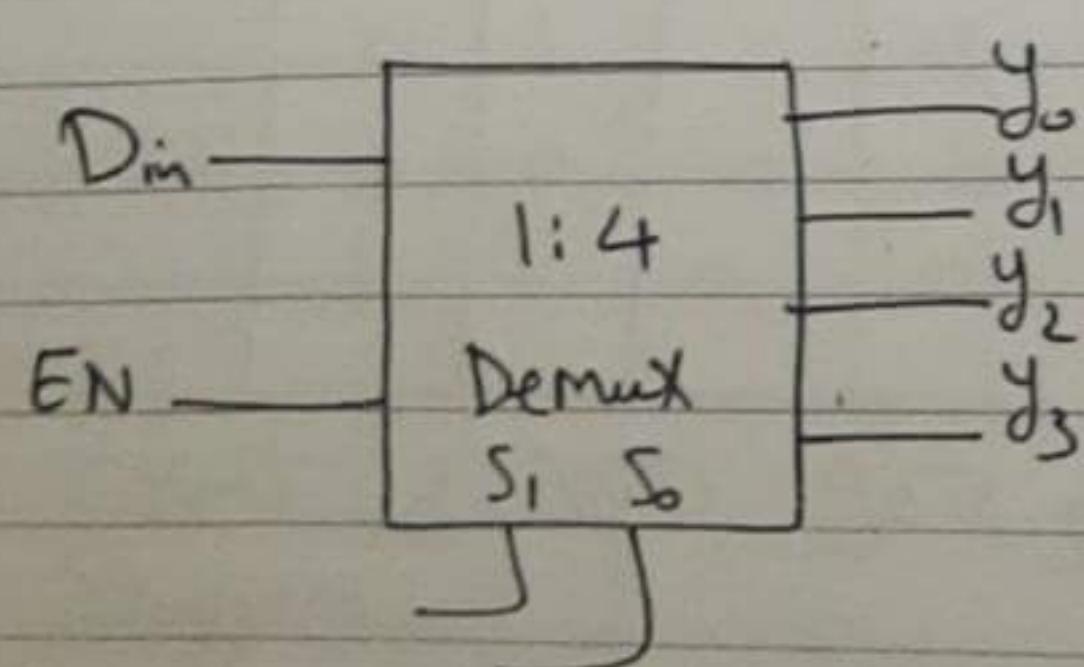
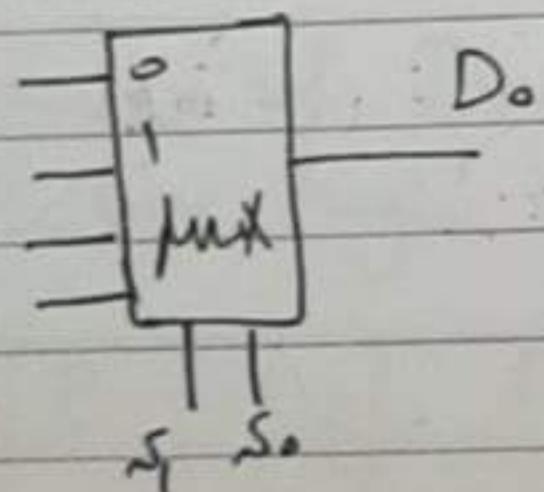
* Demultiplexer:-



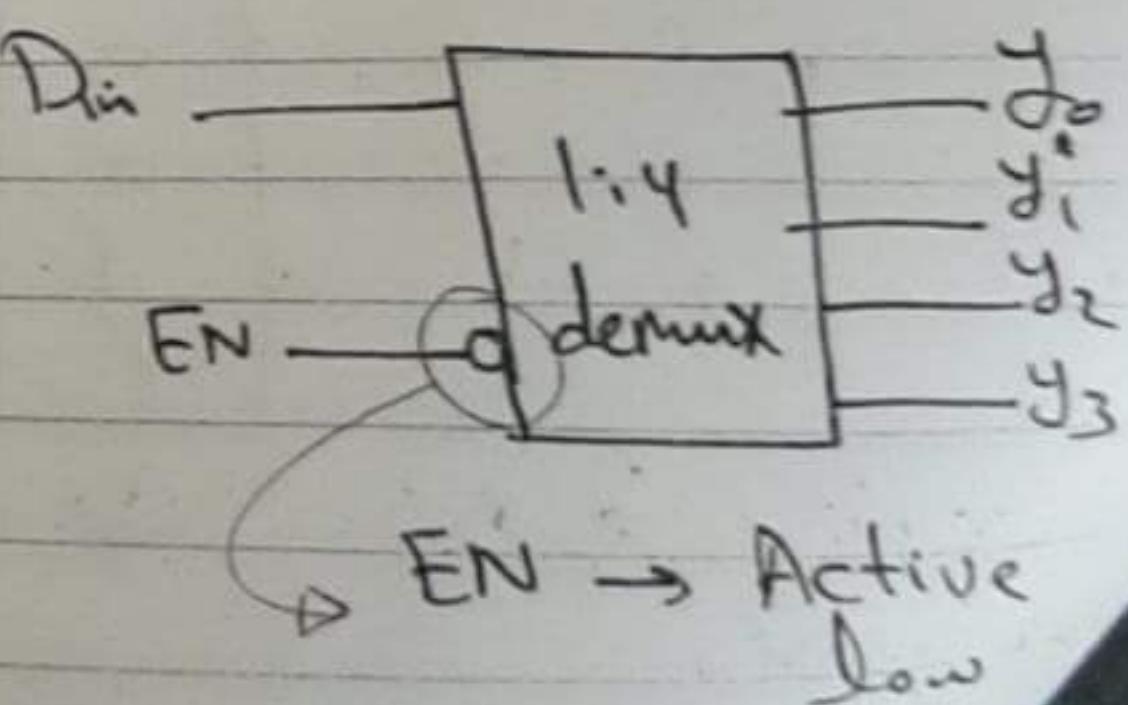
* Logic Circuit of 1X4 Demux.



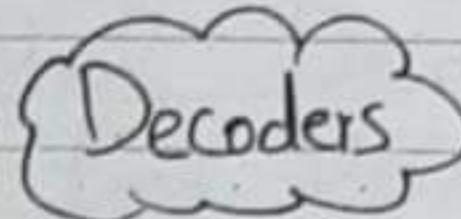
* Symbol



EN → Active high



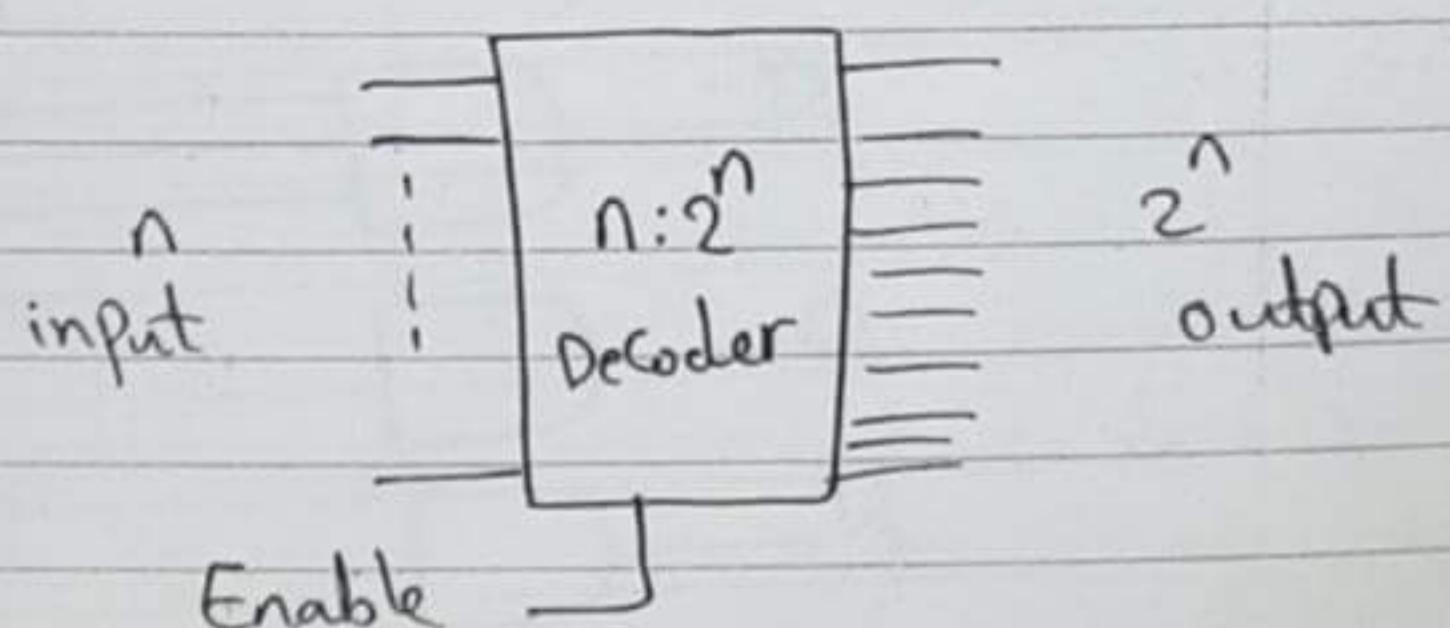
* Mux \rightarrow Multiple input, Single output logic circuit.

*  Decoders

Multiple input, multiple output logic circuit

سُعْيَ الْمَاءِ رَسْفَنْ

Security



$ABC \rightarrow 0000 \ 0000$

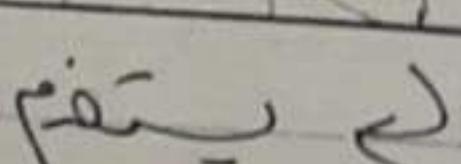
--- 2 octal
Decoder

2 Seven Segment 2 Binary decoder

Selection lines active high

* Function table of Decoders (2:4 line decoder)
(Active high Decoder).

A	B	D ₀	D ₁	D ₂	D ₃
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Circuit of AND gate 
Diagram

Code word
 $01 \rightarrow 0100$

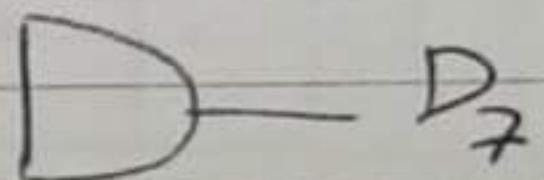
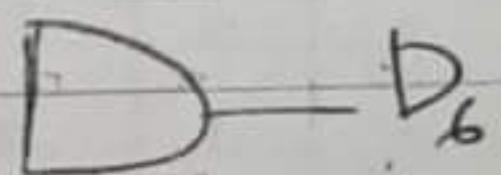
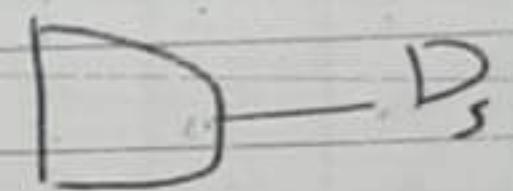
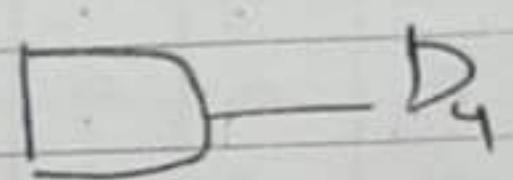
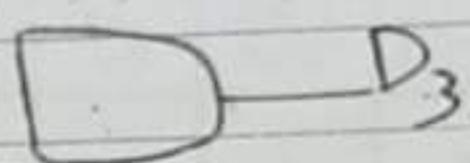
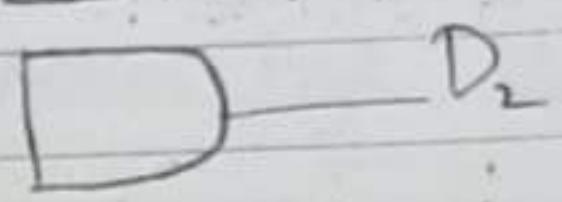
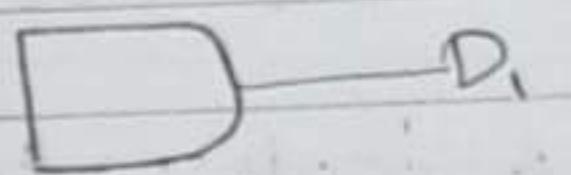
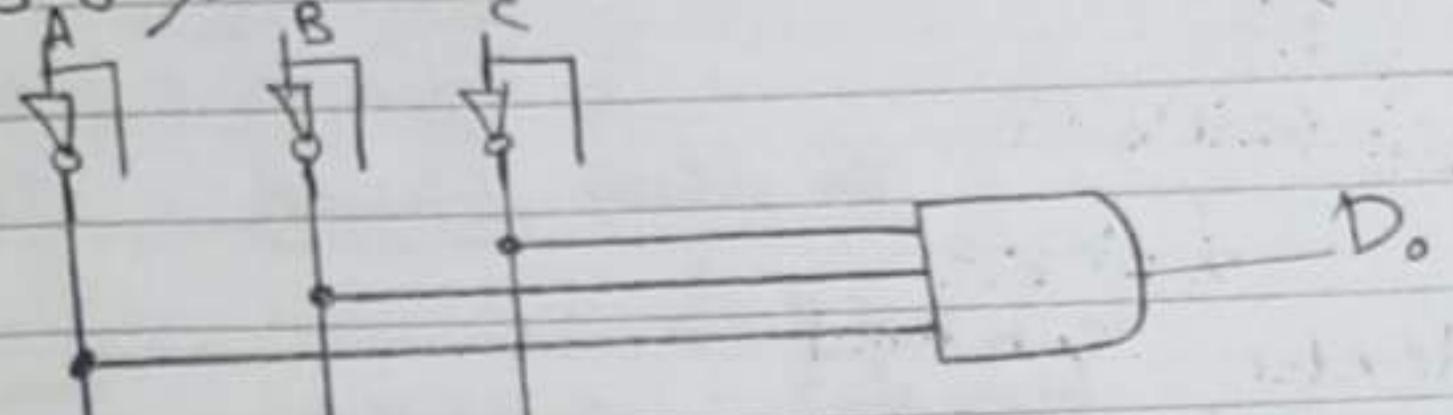
$10 \rightarrow 0010$

$11 \rightarrow 0001$

Active low $\xrightarrow{\text{uses}}$ NAND gate in Circuit diagram.

* octal Decoder
3:8 line Decoder

(8 AND gate 8 line)



)F

)F